REMARKS

Applicant submits this paper in response to the Office Action mailed on December 1, 2005, in which claims 1 and 5-8 were rejected.

Applicant filed a Request for Continued Examination together with an Amendment on November 7, 2005. In response thereto, the Examiner issued a new grounds of rejection in the Office Action of December 1, 2005.

In Item 3 of the December 1, 2005 Office Action, claims 1 and 5-8 were rejected under 35 U.S.C. 102(b) as being anticipated by Pilo (US 5,343,428). Claim 1 is directed to:

> 1. A sense amplifier, comprising:
> a sampling circuit receiving an input signal to the sense amplifier;
> a reference node operable to store a reference signal corresponding to the input data, the reference signal serving as a reference voltage of the sense amplifier; and
> a timing circuit activating the sampling circuit a predetermined interval before measurement of the input signal is initiated, the sampling circuit admitting the input signal to the reference node thereby.

In Item 3 of the 12/1/05 Office Action, the Examiner asserts that the "reference node" of claim 1 "reads on either node 102." Applicant assumes that the Examiner intended to assert that the reference node reads on either node 101 or 102 of Pilo. Applicant respectfully disagrees with this assertion. Nodes 101 and 102 of Pilo are not reference nodes of the differential amplifier 25, operable to store a reference signal. The terms "reference node," "reference signal" and "reference voltage" are terms of art that are well understood by those of skill in the art of sensing amplifiers. Furthermore, claim 1 clarifies that "the reference signal serv(es) as a reference voltage of the sense amplifier." In the Office Action dated May 3, 2005, the Examiner argues that nodes 101 and 102 of Pilo are reference nodes "because they are performing the same function/operation as applicant's 'reference' nodes, i.e., if applicant's node 1021 is a reference node, then so too is node 101 (or 102) of Pilo." Applicant respectfully submits that nodes 101 and 102 of Pilo do not, in fact, perform the same function/operation as the reference node of claim 1 or reference node 1021 in FIG. 10. Specifically, nodes 101 and 102 do not function to store a reference voltage of the differential amplifier 25. Furthermore, Applicant submits that

because differential amplifier 25 of Pilo is a *differential* amplifier, it does not make use of a reference voltage at all. Instead, the differential amplifier 25 compares the two input signals to each other, rather than comparing an input signal to a reference signal. Therefore, Applicant respectfully submits that nodes 101 and 102 of Pilo are not reference nodes. Similarly, the "sampling circuit" of Pilo does not admit the input signal (MUXLAT or MUXLAT*) to a reference node. Therefore, Applicant submits that claim 1 is not anticipated by Pilo.

Also in Item 3 of the 12/1/05 Office Action, the Examiner asserts that the "timing circuit" of claim 1 "reads on the (unillustrated) circuitry which outputs the clock signal CLK." The timing circuit of claim 1 "activat(es) the sampling circuit a predetermined interval before measurement of the input signal is initiated, the sampling circuit admitting the input signal to the reference node thereby." The Examiner alleges that the circuitry in Pilo that outputs the clock signal CLK "activates the sampling circuit prior to measurement of the input signal MUXLAT." Applicant disagrees with this statement; but more importantly, the statement mischaracterizes claim 1. Claim 1 states that the timing circuit "activat(es) the sampling circuit a predetermined interval before measurement of the input signal *is initiated*," as opposed to activating the sampling circuit a predetermined interval before measurement of the input signal *is completed.* Applicant submits that it is precisely the CLK signal of Pilo that initiates the measurement of the input signal. Therefore, the CLK signal of Pilo cannot be said to activate the sampling circuit a predetermined time before measurement of the input signal is initiated. Put another way, in Pilo, activating the "sampling circuit" and initiating the measurement of the input signal are one and the same. Referring to FIG. 2 and column 7, lines 51-60, of Pilo, the transition of the CLK signal from low to high at time t4 causes the transfer gates 43 and 52 (the "sampling circuit") to become conductive, allowing the input signals MUXLAT and MUXLAT* to propagate through the BICMOS sense amplifier 20, as indicated by the successive transitions of the voltage levels of node 101, node 102, node 103, node 104 and output signals PED and PED* after time t4. Thus, the transition of the CLK signal from low to high activates the sampling circuit and initiates the measurement of the input signals. It is the transition of the CLK signal from low to high that causes the input signals MUXLAT and MUXLAT* to be admitted to the differential amplifier 25, as indicated by the transitions of the voltage levels of node 101, node 102, node

103, node 104 and output signals PED and PED* after time t4. Of course, the value of the output signals PED and PED* do not change instantaneously upon the CLK transition (though nearly so); the propagation of the signal through nodes 101 and 102, and then through nodes 103 and 104, takes a finite (though very small) amount of time. But claim 1 says that the timing circuit activates the sampling circuit "a predetermined interval before measurement of the input signal is *initiated*," as opposed to "a predetermined interval before measurement of the input signal is *completed*." In Pilo, the activation of the "sampling circuit" (transfer gates 43 and 52) and the initiation of the measurement of the input signal are one and the same. Therefore, the timing circuit clearly does not activate the sampling circuit a predetermined interval before measurement of the input signal is initiated, as called for in claim 1. Thus Applicant submits that claim 1 further differentiates over Pilo.

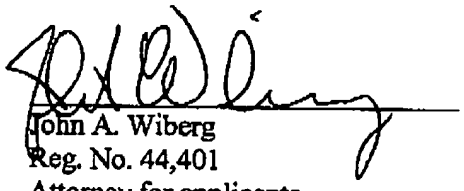
Claim 5 is similar to claim 1 and was rejected under the same grounds as claim 1. Therefore, Applicant submits that claim 5, and claims 6-8 depending therefrom, are not anticipated by Pilo for at least the reasons set forth above with respect to claim 1.

In view of the foregoing, Applicant respectfully requests reconsideration and allowance of claims 1 and 5-8.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Date: 3/1/06

Respectfully submitted,



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